

09/28/00


jc925 U.S. PTO
09/28/00

Please type a plus sign (+) inside this box -

+

PTO/SB/05 (1/98)
Approved for use through 09/30/2000 OMB 0651-0032
Patent and Trademark Office U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

UTILITY PATENT APPLICATION TRANSMITTAL		Attorney Docket No. 0756-2210	
		First Inventor or Application Identifier: Shunpei YAMAZAKI et al.	
		Title: ORGANIC ELECTROLUMINESCENT DISPLAY DEVICE	
(Only for new nonprovisional applications under 37 CFR 1.53(b))		Express Mail Label No.	
APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents.		ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231	
<p>1 <input type="checkbox"/> Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original, and a duplicate for fee processing)</p> <p>2 <input checked="" type="checkbox"/> Specification Total Pages [26] (preferred arrangement set forth below)</p> <ul style="list-style-type: none">- Descriptive title of the invention- Cross References to Related Applications- Statement Regarding Fed sponsored R & D- Reference to Microfiche Appendix- Background of the Invention- Brief Summary of the Invention- Brief Description of the Drawings (if filed)- Detailed Description- Claim(s)- Abstract of the Disclosure <p>3 <input checked="" type="checkbox"/> Drawing(s) (35 USC 113) Total Sheets [6]</p> <p>4 <input type="checkbox"/> Oath or Declaration Total Pages []</p> <ul style="list-style-type: none">a <input type="checkbox"/> Newly executed (original or copy)b <input type="checkbox"/> Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 17 completed) [Note Box 5 below]i. <input type="checkbox"/> DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b) <p>5 <input type="checkbox"/> Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein</p>		<p>6. <input type="checkbox"/> Microfiche Computer Program (Appendix)</p> <p>7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)</p> <ul style="list-style-type: none">a. <input type="checkbox"/> Computer Readable Copyb. <input type="checkbox"/> Paper Copy (identical to computer copy)c. <input type="checkbox"/> Statement verifying identity of above copies	
ACCOMPANYING APPLICATION PARTS			
<p>8 <input type="checkbox"/> Assignment Papers (cover sheet & document(s))</p> <p>9. <input type="checkbox"/> 37 CFR 3.73(b) Statement [] Power of Attorney (when there is an assignee)</p> <p>10. <input type="checkbox"/> English Translation Document (if applicable)</p> <p>11. <input type="checkbox"/> Information Disclosure Statement [] Copies of IDS (IDS)/PTO-1449 Citations</p> <p>12 <input type="checkbox"/> Preliminary Amendment</p> <p>13 <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) (Should be specifically itemized)</p> <p>14. <input type="checkbox"/> *Small Entity [] Statement filed in prior application, Statement(s) Status still proper and desired (PTO/SB/09-12)</p> <p>15. <input checked="" type="checkbox"/> Certified Copy of Japanese Priority Document No. 11-279870 Filed September 30, 1999</p> <p>16 <input type="checkbox"/> Other.</p> <p>*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon</p>			
17. If a CONTINUING APPLICATION , check appropriate box, and supply the requisite information below and in a preliminary amendment: Prior application information: Examiner: Group/Art Unit:			
18. CORRESPONDENCE ADDRESS			
<input checked="" type="checkbox"/> Customer Number or Bar Code Label Customer No. 22204 or <input type="checkbox"/> Correspondence address below			
(Insert Customer No. or Attach bar code label here)			
Name Eric J. Robinson Firm NIXON PEABODY LLP Address 8180 Greensboro Drive, Suite 800 City McLean State VA Zip Code 22102 Country U S A Telephone (703) 790-9110 FAX (703) 883-0370			
Name: Eric J. Robinson		Registration No. 38,285	
Signature 		Date: September 28, 2000	

Burden Hour Statement This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

A
jc925 U.S. PTO
09/28/00
09/28/00

	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2
--	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	---

Field of the Invention:

The present invention relates to a semiconductor device having a circuit based on insulated-gate field effect transistors in which a single-crystal semiconductor is used for an active layer, and a method of fabricating the semiconductor device. More particularly, the present invention is well suited for applications to an electrooptic device which is typified by an organic electroluminescent display device wherein the same substrate is overlaid with a pixel unit and driver circuits disposed around the pixel unit, and to an electronic apparatus in which the electrooptic device is installed. Incidentally, here in this specification, the expression "semiconductor device" is intended to signify general devices which function by utilizing semiconductor properties, and it shall cover within its category the electrooptic device and the electronic equipment including this electrooptic device.

In the field of flat display devices (flat panel displays) typified by liquid-crystal display devices, organic EL (electroluminescent) display devices, etc.,

005504934960

there has been known technology wherein a display device of active matrix type is fabricated by employing insulated-gate field effect transistors (hereinbelow, the "field effect transistors" shall be abbreviated to "FETs") formed on a single-crystal semiconductor substrate. Unlike in a case where a display device of active matrix type is fabricated by forming thin-film transistors (hereinbelow, abbreviated to "TFTs") on a glass substrate or a quartz substrate, the technology has had the advantage that techniques fostered in the field of large-scale integrated circuits (LSIs) are applicable as they are, and that the FETs of high performance which are capable of low-voltage drive at high speed can be integrated and formed at a high density on the substrate. On the other hand, however, it has been considered the disadvantage of the technology that the display device is restricted to one of reflection type or spontaneous luminescence type because the substrate is opaque to visible light, or that the single-crystal semiconductor substrate is restricted to sizes available on the market.

In the technological trends toward higher image quality and full digitization in the field of the display devices, the enhancements of performances required of the active matrix type display device have inevitably

heightened. The active matrix type display device is so constructed that transistors (such as TFTs or FETs) in the number of several tens to several millions are arranged in a pixel unit for displaying an image, and that pixel electrodes are respectively connected to the transistors. In operation, the image is displayed in such a way that voltages to be applied to respective pixels are controlled by the switching functions of the corresponding transistors, whereby some of EL elements are caused to luminesce. In the organic EL display device, when the switching transistors disposed in the respective pixels are turned ON, currents are caused to flow through current controlling transistors by signals generated in accordance with image data, whereby the EL elements luminesce spontaneously.

However, an organic EL layer which serves as the basic portion of the organic EL display device is very liable to oxidize, and it easily deteriorates in the presence of a slight amount of oxygen. Besides, it has a low becomes a cause for resistance to heat, and this also is a factor promoting oxidation. The liability to oxidize is the cause of a short lifetime of the organic EL element, and has formed a serious obstacle in putting this element into practical use.

layer; characterized in that the single-crystal semiconductor substrate is held in a vacant space which is defined by a bed plate and a cover plate formed of an insulating material, and a packing material for bonding the bed and cover plates; that the cover plate is formed of a transparent member in its area which lies over the pixel unit; and that the vacant space is filled with an inert gas and a drying agent.

A single-crystal silicon substrate can be favorably employed as the single-crystal semiconductor substrate. Besides, the vacant space should preferably be filled with an inert gas selected from the group consisting of helium, argon, krypton, xenon and nitrogen, and a drying agent selected from the group consisting of barium oxide and silica gel.

BRIEF DESCRIPTION OF THE DRAWINGS:

Fig. 1 is a sectional view of an organic EL display device of active matrix type;

Figs. 2(A) and 2(B) are diagrams showing the top plan structure and circuit arrangement of a pixel unit in the organic EL display device, respectively;

Fig. 3 is a top plan view of the active matrix type organic EL display device;

Fig. 4 is a sectional view showing the internal

construction of the organic EL display device;

Fig. 5 is a perspective view showing the construction of a goggle type display device in which the organic EL display devices are installed; and

Figs. 6(A) and 6(B) are sectional views of the goggle type display device in which the organic EL display devices are installed.

PREFERRED EMBODIMENTS OF THE INVENTION:

First, an organic EL display device according to the present invention will be described with reference to Fig. 1. The organic EL display device according to the present invention has such a structure that a pixel unit and driver circuits around the pixel unit are disposed using field effect transistors (FETs) of insulated gate type which are formed on a single-crystal semiconductor substrate (for example, single-crystal silicon substrate).

A substrate 101 is made of single-crystal silicon having a comparatively high resistance (for example, one of n-type at about 10 [Ω cm]), and a p-well 102 and n-wells 103 ~ 105 are formed in self-alignment therein. Adjacent FETs are isolated by a field oxide film 106. In forming the field oxide film 106, channel stoppers may be formed by introducing boron (B) into the selected parts of the

substrate 101 in accordance with ion implantation.

Gate insulating films 110, 116, 122 and 128 are formed by thermal oxidation. Gates 111, 117, 123 and 129 consist of polycrystalline silicon layers 111a, 117a, 123a and 129a formed from a polycrystalline silicon film deposited to a thickness of 100 ~ 300 [nm] by CVD, and silicide layers 111b, 117b, 123b and 129b formed thereon to a thickness of 50 ~ 300 [nm], respectively. The polycrystalline silicon layers may be doped with phosphorus (P) at a concentration of 10^{21} [/cm³] or so beforehand in order to lower the resistance thereof, or an n-type impurity at a high concentration may be diffused after the polycrystalline silicon film has been formed. Applicable as the material of the silicide layers is any of molybdenum silicide (MoSi_x), tungsten silicide (WSi_x), tantalum silicide (TaSi_x), titanium silicide (TiSi_x), etc., and the silicide layers may well be formed in accordance with a known method.

The lightly-doped drain (LDD) regions 107 of a p-channel FET 201 are doped with boron (B) at a dose of $1 \times 10^{13} \sim 1 \times 10^{14}$ [/cm²] as an impurity element which bestows the conductivity type of p-type. On the other hand, the LDD regions 113 of an n-channel FET 202, and those 119 and 125 of a switching FET 203 and a current controlling FET 204 made up of n-channel FETs are doped

with phosphorus (P) or arsenic (As) as the impurity element which bestows n-type conductivity, at a dose similar to that of p-type. These LDD regions are respectively formed in self-alignment in accordance with ion implantation or ion doping by employing the corresponding gates as masks.

Side wall spacers 112, 118, 124 and 130 are formed in such a way that, after the formation of the LDD regions, an insulating film such as silicon oxide film or silicon nitride film is formed on the whole surface of the resulting substrate by CVD, and that the insulating film is uniformly etched over the whole area thereof by anisotropic dry etching, so as to be left behind on the side walls of the corresponding gates. The source regions and drain regions of the respective FETs are formed by employing the corresponding side wall spacers as masks. More specifically, the source region 108 and drain region 109 of the p-channel FET 201 is formed by ion-implanting boron (B) at a dose of $5 \times 10^{14} \sim 1 \times 10^{16}$ [/cm²]. The n-channel FET 202, and the switching FET 203 and current controlling FET 204 made up of these n-channel FETs are respectively formed with the source regions 114, 120 and 126 and drain regions 115, 121 and 127 by ion-implanting arsenic (As) at a dose of $5 \times 10^{14} \sim 1 \times 10^{16}$ [/cm²].

A first interlayer insulating film 131 is formed

to a thickness of 100 ~ 2000 nm out of a silicon oxide film, an oxidized silicon nitride film or the like which should preferably be prepared by plasma CVD or low-pressure CVD. Further, the first interlayer insulating film 131 is overlaid with a second interlayer insulating film 132 which is made of phosphosilicate glass (PSG), borosilicate glass (BSG) or phosphoborosilicate glass (PBSG). The second interlayer insulating film 132 is prepared by spin coating or normal-pressure CVD. The prepared film is caused to reflow by a treatment of thermal activation at 700 ~ 900 [°C], which is carried out after the preparation and which serves also as a heat treatment, whereby the surface of the second interlayer insulating film 132 is flattened.

Source wiring lines 133, 135, 137 and 139 and drain wiring lines 134, 136, 138 and 140 are respectively formed after contact holes reaching the source regions and drain regions of the corresponding FETs are formed in the first interlayer insulating film 131 and the flattened film 132. Aluminum (Al) which is usually and often used as a low-resistance material, may be employed for the wiring lines. Alternatively, a multilayer structure consisting of an Al layer and a titanium (Ti) layer may be employed for each of the wiring lines.

A passivation film 141 is formed of a silicon nitride

cathode layers 144 containing a metal of low work function are formed on all the pixel electrodes. Since the cathode layer 144 is as thin as a few nm or so, whether a true layer is formed or it exists sporadically in the shape of islands is unclear, and hence, its contour is indicated by a broken line.

A material which is usable as the cathode layer 144 containing the metal of low work function, is lithium fluoride (LiF), lithium oxide (Li_2O), barium fluoride (BaF_2), barium oxide (BaO), calcium fluoride (CaF_2), calcium oxide (CaO), strontium oxide (SrO) or cesium oxide (Cs_2O). Since the material is insulating, the short-circuiting between the pixel electrodes is not incurred even when the cathode layer 144 is a connecting layer. Of course, a cathode layer made of a known material having conductivity, such as MgAg electrode, can be used as the cathode layer. It is necessary, however, to form cathodes themselves selectively or to perform patterning, so as to prevent the pixel electrodes from short-circuiting.

An organic EL (electroluminescent) layer 145 is formed on the cathode layer 144 containing the metal of low work function. Although a known material or structure can be employed for the organic EL layer 145, a material capable of white luminescence is used in the present

invention. Structurally, the organic EL layer 145 may be formed of nothing but a luminescent layer which offers a site for recombination. If necessary, it is also allowed to stack on this an electron injection layer, an electron transport layer, a hole transport layer, an electron blocking layer, a hole blocking layer or a hole injection layer. Here in this specification, all the layers where carriers are injected, transported or recombined shall be comprehensively called the "organic EL layer".

In addition, the organic EL material used for the organic EL layer 145 is a high-molecular one based on a polymer. For example, the organic EL layer 145 is formed in such a way that PVK (polyvinyl carbazole), Bu-PBD (2-(4'-tert-butylphenyl)-5-(4"-biphenyl)-1, 3, 4-oxadiazole), coumarin 6, DCM 1 (4-dicyanomethylene-2-methyl-6-p-dimethylaminostyryl-4H-pyran), TPB (tetraphenylbutadiene) and Nile red are dissolved in 1, 2-dichloromethane or chloroform, and that a solution thus obtained is applied by spin coating. The substrate structure coated with the solution is rotated at a rotational frequency of about 500 ~ 1000 [rpm] for 20 ~ 60 [seconds], whereby a uniform coating film is formed.

Of course, the coating film is formed after the

organic EL material is refined (typically, by dialyzing) at least 3 times, preferably 5 times or more, thereby to lower the sodium content of this material to 0.1 [ppm] or less (preferably, 0.01 [ppm] or less). Thus, the sodium content of the organic EL layer 349 becomes 0.1 [ppm] or less (preferably, 0.01 [ppm] or less), and the volume resistance thereof becomes $1 \times 10^{11} \sim 1 \times 10^{12}$ [Ωcm] (preferably, $1 \times 10^{12} \sim 1 \times 10^{13}$ [Ωcm]).

The organic EL layer 145 formed in this way is overlaid with a transparent conductive film as an anode layer 146. Usable for the transparent conductive film is a compound (called "ITO") produced from indium oxide and tin oxide, a compound produced from indium oxide and zinc oxide, tin oxide (SnO_2), zinc oxide (ZnO), or the like.

Besides, the anode layer 146 is overlaid with an insulating film as a passivation film 147. The passivation film 147 should preferably be a silicon nitride film or a nitrified silicon oxide film (expressed by " SiO_xN_y ").

The substrate structure completed up to this point in this specification shall be called "active matrix substrate". That is, the "active matrix substrate" is the substrate which is formed with the FETs, the pixel electrodes electrically connected to the FETs, and

organic EL elements including pixel electrodes as the cathodes (capacitors consisting of the cathode layers, the organic EL layer and the anodes).

Fig. 2(A) is a top plan view of the pixel unit of the active matrix substrate, while Fig. 2(B) is a connection diagram of the circuit arrangement of the pixel unit. In actuality, the pixel unit (image display unit) is so constructed that a plurality of pixels are arrayed in the shape of a matrix. Incidentally, a sectional view taken along A - A' in Fig. 2(A) corresponds to the sectional view of the pixel unit in Fig. 1. Accordingly, common reference numerals are indicated in Fig. 1 and Fig. 2(A), both of which may be referred to on occasion. Besides, two pixels are illustrated in the top plan view of Fig. 2(A), and they have the same structure. As shown in Fig. 2(B), two FETs per pixel are disposed for the organic EL element 205. Both the FETs are of n-channel type, and they function as the switching FET 203 and the current controlling FET 204.

In the above way, upon the single-crystal silicon substrate can be formed driver circuits each of which is based on a CMOS circuit configured with a p-channel FET 201 and a n-channel FET 202, and pixel units each of which includes switching FET 203 and current controlling FET 204 formed of n-channel FETs. The driver

circuits based on the CMOS circuits can form, for example, a shift register circuit, a buffer circuit, a sampling circuit, a D/A converter, and a latch circuit. Since such circuits are constructed of the insulated-gate FETs whose active layers are made of single-crystal silicon, they are capable of high-speed operations, and a lower power consumption can be achieved by setting their drive voltages at 3 ~ 5 [V]. By the way, the structures of the FETs explained in this embodiment are nothing more than mere examples, and the FETs need not be restricted to the structures shown in Fig. 1.

Fig. 3 is a top plan view showing an active matrix substrate. Referring to the figure, the active matrix substrate includes a substrate 1000, a pixel unit 1001, data line side driver circuits 1003, and scanning line side driver circuits 1002. Input terminals for the respective driver circuits are pads 1006 for wire bonding which are disposed near the edges of the substrate 1000, and they are connected to the driver circuits via leads 1004 ~ 1005. The pixel unit having a size of from 0.5-inch class to 2.5-inch class is well suited for fabrication.

The active matrix substrate formed with the organic EL layer is sealed in a package in order to be cut off from external shocks, and ambient conditions such as dust and humidity. The shape and scheme of the package are

exemplified in Fig. 4. A bed plate 401 is formed of an insulating material such as ceramics, and the active matrix substrate 413 formed with the organic EL layer is fixed thereon by a low-melting glass or metallized layer 402. The active matrix substrate 413 is connected with an external circuit by a lead frame 404, which is connected with the active matrix substrate 413 by wire pieces 412 of gold (Au) through pads 410 for wire bonding.

The active matrix substrate 413 is sealed with a cover ceramic plate 405. The ceramic cover plate 405 is bonded with the bed plate 401 by a binder layer 404. Pyroceram cement, bismuth oxide-based glass, lead oxide-based glass, or the like is used for the binder layer 404. A window member 406 made of a transparent quartz plate, a transparent glass plate or the like is mounted and fixed with adhesives 407 in an area where the cover plate 405 formed of the ceramics or the like insulating material similarly to the bed plate 401 lies over the pixel unit of the active matrix substrate 413. In this way, the active matrix substrate 413 formed with the organic EL layer is enclosed, and a vacant space 414 is formed. Further, the vacant space 414 should desirably be filled with an inert gas (such as argon, helium, krypton, xenon or nitrogen) or have a drying agent (such as barium oxide) put therein. In this way it is possible to suppress

the deterioration of the EL element attributed to moisture etc.

Although not shown in this embodiment, a color display can also be constructed by disposing color filters or black matrix layers (light intercepting layers) on the organic EL layer in correspondence with the individual pixels formed from the organic EL layer of the active matrix substrate. Alternatively, color filters may well be disposed at the window 406 shown in Fig. 4.

In the state shown in Fig. 4 as described above, the lead frame 403 is connected to the terminals of the external equipment, whereby an image signal etc. can be inputted to display an image on the pixel unit. Here in this specification, an article which is brought into a state where it is capable of displaying an image, by attaching a lead frame to an external circuit, is defined as an "organic EL display device".

Now, there will be described a practicable example in which an organic EL display device of active matrix type is applied to a goggle type display device. Fig. 5 shows a schematic view of the goggle type display device in this example. The goggle type display device main body 3600 is furnished with two, right and left display units, which are constructed of organic EL display devices 3602R, 3602L, circuit boards 3603R, 3603L and lenses 3601R,

3601L.

Fig. 6(A) shows a sectional view of part A indicated in Fig. 5, while Fig. 6(B) shows an enlarged view of part B indicated in Fig. 6(A). As shown in Figs. 6(A) and 6(B), in this example, in the goggle type display device 3600 the organic EL display device 3602R mounted on the lens 3601R is connected to the circuit board 3603R equipped with a signal control circuit etc., through a lead frame 3606R. Light luminescing from the organic EL display device 3602R arrives at the eyeball 3604R of a user via an optical path indicated by arrows in Fig. 6(A), whereby the user can recognize an image.

The organic EL display device has a wide view angle owing to its spontaneous luminescence. When applied to the goggle type display device, the organic EL display is not spoilt even if the relative positions of this display device and an observer's eye have deviated.

The present invention brings forth an effect as stated below:

A single-crystal semiconductor substrate which is formed with insulated-gate field effect transistors and an EL layer, is held in a vacant space which is defined by a bed plate and a cover plate formed of an insulating material, and a packing material for bonding the bed and cover plates, and the vacant space is filled with an inert

gas and a drying agent, whereby the oxidation of the EL layer can be prevented to provide an organic EL display device of high reliability.

substrate;

an organic EL layer provided over said insulated gate field effect transistor;

a bed plate and a cover plate formed of an insulating material;

a packing material for bonding the bed and cover plates,

wherein the single crystal semiconductor substrate is held in a vacant space which is defined by the bed plate and the cover plate and the packing material,

wherein the cover plate comprises a transparent material in a region of the cover plate overlapping with the pixel section, and

wherein the vacant space is filled with an inert gas and a drying agent.

4. A device according to claim 3 wherein said organic EL display device is employed for a display portion of a goggle type display device.

5. An active matrix type organic EL display device comprising:

an insulated gate field effect transistor provided in a pixel section on a single crystal semiconductor substrate;

on a single crystal semiconductor substrate;

an organic EL layer provided over said insulated gate field effect transistor;

a bed plate and a cover plate formed of an insulating material;

a binder layer for bonding the bed and cover plates,

wherein the single crystal semiconductor substrate is held in a vacant space which is defined by the bed plate and the cover plate and the binder layer, and

wherein the vacant space is filled with an inert gas and a drying agent.

8. A device according to claim 7 wherein said organic EL display device is employed for a display portion of a goggle type display device.

9. An active matrix type organic EL display device comprising:

an insulated gate field effect transistor provided in a pixel section on a single crystal semiconductor substrate;

an organic EL layer provided over said insulated gate field effect transistor;

a bed plate and a cover plate formed of an insulating material;

a binder layer for bonding the bed and cover plates,
wherein the single crystal semiconductor substrate
is held in a vacant space which is defined by the bed
plate and the cover plate and the binder layer,

wherein the cover plate comprises a transparent
material in a region of the cover plate overlapping with
the pixel section, and

wherein the vacant space is filled with an inert
gas and a drying agent.

10. A device according to claim 9 wherein said organic
EL display device is employed for a display portion of
a goggle type display device.

11. An active matrix type organic EL display device
comprising:

an insulated gate field effect transistor provided
in a pixel section on a single crystal semiconductor
substrate;

an organic EL layer provided over said insulated
gate field effect transistor;

a bed plate and a cover plate formed of a ceramics
material;

a binder layer for bonding the bed and cover plates,
wherein the single crystal semiconductor substrate

is held in a vacant space which is defined by the bed plate and the cover plate and the binder layer,

wherein the cover plate comprises a transparent material in a region of the cover plate overlapping with the pixel section, and

wherein the vacant space is filled with an inert gas selected from the group consisting of helium, argon, krypton, xenon and nitrogen, and is filled with a drying agent selected from the group consisting of barium oxide and silica gel.

12. A device according to claim 11 wherein said organic EL display device is employed for a display portion of a goggle type display device.

ABSTRACT

An organic EL display device of active matrix type wherein insulated-gate field effect transistors formed on a single-crystal semiconductor substrate are overlaid with an organic EL layer; characterized in that the single-crystal semiconductor substrate (413 in Fig. 4) is held in a vacant space (414) which is defined by a bed plate (401) and a cover plate (405) formed of an insulating material, and a packing material (404) for bonding the bed and cover plates; and that the vacant space (414) is filled with an inert gas and a drying agent, whereby the organic EL layer is prevented from oxidizing.

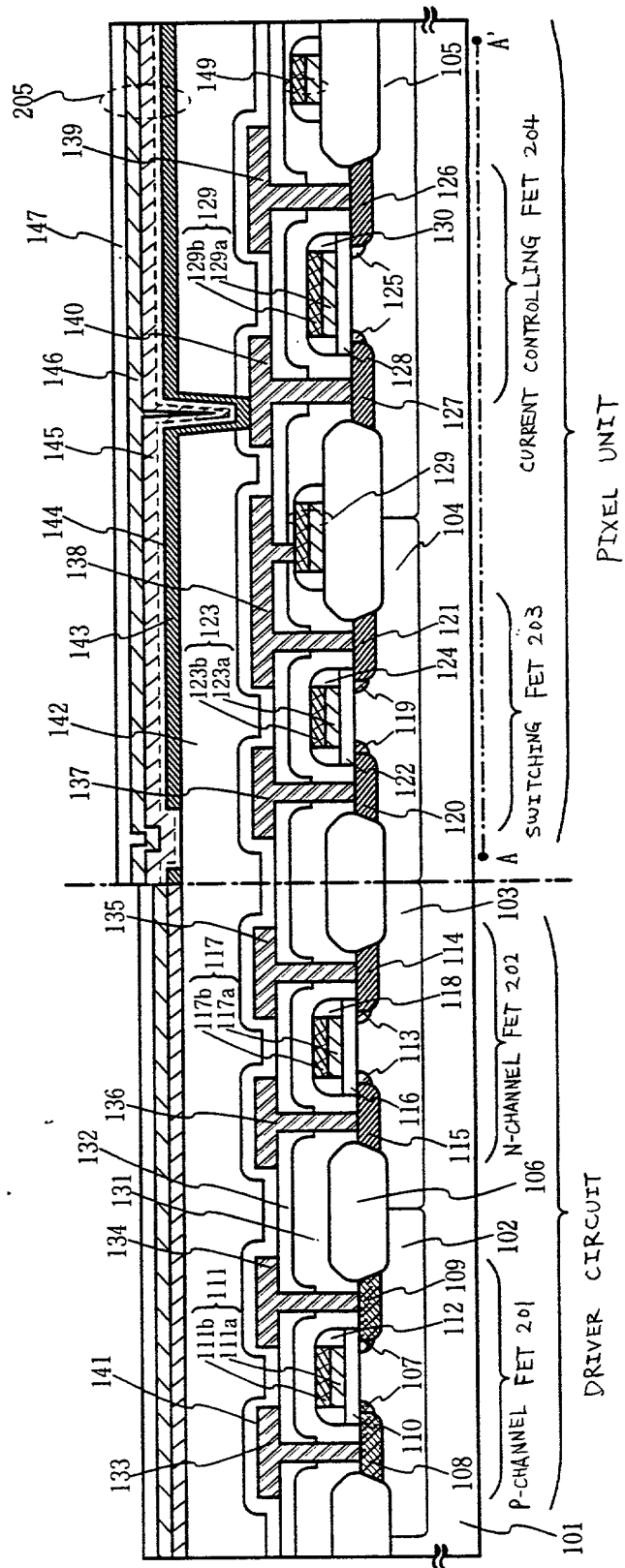
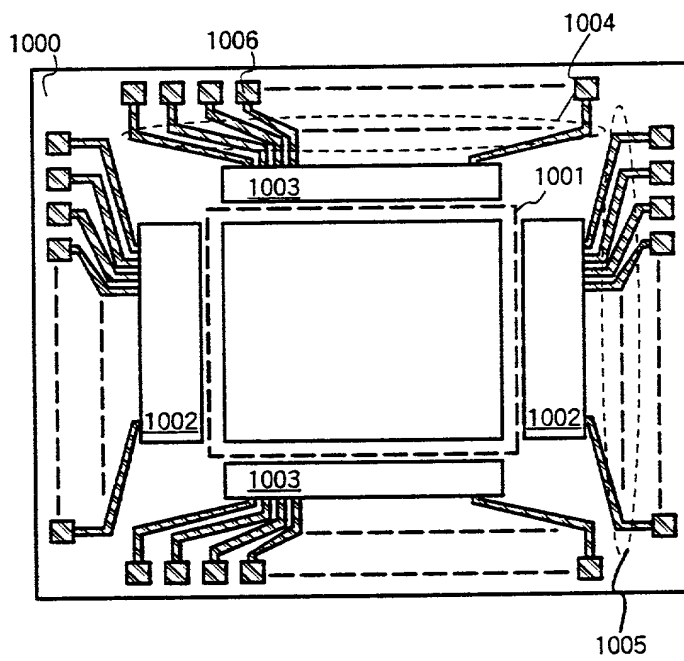


Fig. 3



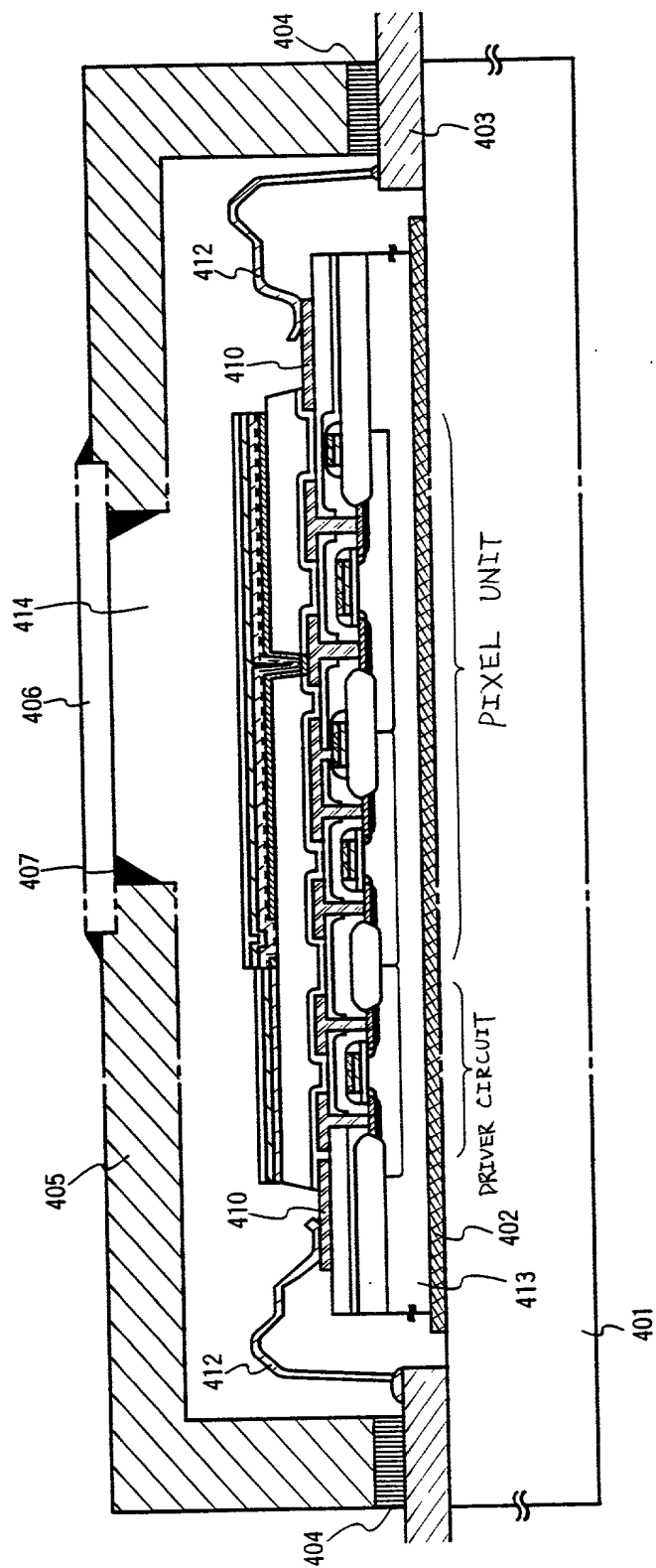


Fig. 4

